STIC Search Report
EIC 2800

STIC Database Tracking Number: 212418

TO: Tuan Dinh **Location: JEF 10D51** **Art Unit : 2841** **Thursday, January 11, 2007** **Case Serial Number: 09/945394**	**From: Michael Obinna** **Location: EIC 2800** **JEF4B68** **Phone: 272-2663** **michael.obinna@uspto.gov**

Search Notes

RE: **Circuit Board plane interleave apparatus and method**

Examiner Dinh,

Attached are edited search results from the patent and non-patent databases.

The tagged items are some of the results worth your review.

I recommend that you browse all the results.

If you would like more searching on this case, or if you have questions or comments, please let me know.

Respectfully,

Michael Obinna

212418 Hand Search

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 1/26/2006 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 22511.

SPE. 2831/2841
1-10-07

Date 1/9/06 Serial # 09/945,394 Priority Application Date 8/30/01

Your Name Tuan Dinh Examiner # 77082

AU 2841 Phone 571-272-1929 Room Jeff 10D51

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search request form, please prioritize the searches in order of need.

Where have you searched so far on this case?
Circle: (USPT) DWPI (EPO Abs) (JPO Abs) IBM TDB
Other: _____

What relevant art have you found so far? Please attach citations or Information Disclosure Statements.
Kumagai et al (US 6,147,573) and please check on 892 form

What types of references would you like? Please checkmark:

Primary Refs ____ Nonpatent Literature ____ Teaching Refs ____
Secondary Refs ____ Foreign Patents ____ Other ____

Is this a "Fast & Focused Search" request? (Circle One) YES NO

A "Fast & Focused Search" is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2800 and on the STIC NPL Web Page at http://uspto-a-pattr-2/siraapps/stic/npl/nplsearch.htm

JAN 10

Rush

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

a) First conductive layer having plurality of widths
b) Second Conductive layer having a second width
First layer and second layer engaged together
and second width is overlaped with the first widths.

Thanks.
TD
571-272-1929
Jeff-10D51

Staff Use Only

Searcher: Michael Obeid
Searcher Phone: 571-272-2663
Searcher Location: STIC-EIC2800, JEF-4B68
Date Searcher Picked Up: 1/10/2007
Date Completed: 1/11/2007
Searcher Prep/Rev Time: 100
Online Time: 118

Type of Search

Structure (#) ____
Bibliographic ✓
Litigation ____
Fulltext ____
Patent Family ____
Other ____

Vendors

STN ✓
Dialog ✓
Questel/Orbit ____
Lexis-Nexis ____
WWW/Internet ____
Other ____

1/11/2007 11:53:30 AM
1/11/2007 12:52:41 PM

[File 2] INSPEC 1898-2006/Jan W2
[File 6] NTIS 1964-2006/Jan W4
[File 8] Ei Compendex(R) 1970-2006/Jan W4
[File 34] SciSearch(R) Cited Ref Sci 1990-2006/Jan W4
[File 434] SciSearch(R) Cited Ref Sci 1974-1989/Dec
[File 35] Dissertation Abs Online 1861-2006/Jan
[File 65] Inside Conferences 1993-2006/Jan W5
[File 94] JICST-EPlus 1985-2006/Nov W3
[File 99] Wilson Appl. Sci & Tech Abs 1983-2006/Apr
[File 144] Pascal 1973-2006/Jan W2
[File 23] CSA Technology Research Database 1963-2006/Jan
[File 103] Energy SciTec 1974-2006/Jan B1
[File 31] World Surface Coatings Abs 1976-2006/Jan
[File 95] TEME-Technology & Management 1989-2006/Jan W5
[File 56] Computer and Information Systems Abstracts 1966-2006/Aug
[File 57] Electronics & Communications Abstracts 1966-2006/Aug
[File 68] Solid State & Superconductivity Abstracts 1966-2006/Jan
[File 60] ANTE: Abstracts in New Tech & Engineer 1966-2006/Jan
[File 293] Engineered Materials Abstracts 1966-2006/Jan
[File 239] Mathsci 1940-2005/Feb
[File 256] TECINFOSOURCE 82-2005/DEC

Set Items Description
S1 5579952 S (CIRCUIT????? OR CHIP OR IC OR I()C OR INTEGRATED()CIRCUIT???)(2N)BOARD OR SEMICONDUCTOR? ? OR SEMI()CONDUCTOR? ? OR PCB? ? OR P()C()B OR TAB? ? OR T()A()B OR PRINT????()CIRCUIT()BOARD? ? OR CIRCUIT???()BOARD? ? OR LOAD()BOARD? ? OR LOADBOARD? ? OR LSI? ? OR L()S()I OR ASIC? ? OR A()S()I()C OR ELECTRON???()DEVICE? ? OR PRINT???()CIRCUIT??? OR IC? ? OR I()C OR INTEGRAT????()CIRCUIT??? OR CHIP? ? OR WAFER??? OR MICROCHIP? ? OR MICRO()CHIP? ? OR VLSI? ? OR FLEX?????(3N)CIRCUIT OR FLEX?????? OR (LEAD? ? OR WIRE? ? OR WIRING OR LINE? ? OR TRAC????? OR INTEGRAT?????)(3N)FLEX??????

S2 40934187 S FIRST???? OR ONE OR 1ST OR SECOND????? OR TWO OR 2 OR BOTH OR EACH OR 2ND OR DOUBL??? OR COUPL???? OR ANOTHER OR DUAL????? OR PAIR???? OR TWIN?????

S3 642721 S (CONDUCT???? OR HEAT??? OR THERM??????? OR ELECTRIC????)(3N)(LAYER???? OR FILM???? OR COAT???? OR COVER??????? OR COVER()COAT???? OR SHEET??? OR LAMIN???? OR OVERLAY??????? OR OVER()LAY????? OR COVER()LAY??????)

S4 15617832 S INTERSTIC????? OR AREA OR SPAC???? OR REGION???? OR BREAK???? OR GAP OR GAPS OR APERTURE OR HOLE? ? OR ORIFICE? ? OR OPEN???????? OR CAVIT??????? OR PERFORAT????? OR WINDOW????

S5 3302564 S (PLURAL????? OR MANY OR MULTI?????? OR DIFFER?????? OR NUMBER?????? OR NUMEROUS OR VARI?????????? OR SEVERAL OR DIVERS?????? OR SET OR CLUSTER????)(3N)(WIDTH? ? OR BREADTH OR THICK???? OR BROAD???? OR DIMENSION OR SHAP???? OR SIZE? ?) OR WIDTH OR BREADTH OR THICK????

S6 3487314 S DIELECTRIC OR DIELEC OR CAPACIT????? OR INSULAT????? OR NONCONDUCT????? OR NON()CONDUCT????

S7 339975 S OVERHANG???? OR OVER()(HANG???? OR LAP OR LAPS OR LIES OR LIE) OR OVERLAP???? OR OVERLIE

S8 3048626 S ENGAG????? OR INTERCONNECT??? OR MESH???? OR INTERLOCK???? OR INTER()LOCK???? OR INTER()CONNECT??? OR INTERSECT???? OR JOIN???? OR LOCK????

S9 0 S S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7 AND S8
S10 5893 S S1 AND S2 AND S3 AND S5 AND S6
S11 17 S S10 AND S7
S12 14 RD (unique items)
S13 440 S S10 AND S8
S14 180 S S13 AND S4

S15 2 S S14 AND (SEVERAL??? OR PLURAL???? OR VARI????)(3N)(CIRCUIT???? OR CHIP OR MICROCHIP)

S16 2 RD (unique items)

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S17      1490   S S1(3N)S4 AND S3 AND S5

S18         3   S S17 AND (SEVERAL??? OR PLURAL???? OR VARI????)(3N)(CIRCUIT???? OR CHIP OR
MICROCHIP)

S19         3   RD  (unique items)
S20         0   S S17 AND S6 AND S7 AND S8
S21       395   S S17 AND S6
S22         1   S S21 AND S7
S23        40   S S21 AND S8
S24        34   S S23 AND S2

S25         1   S S24 AND PARALLEL????

S26     29351   S S1(3N)(SEVERAL??? OR PLURAL???? OR VARI????)(3N)(CIRCUIT???? OR CHIP OR
MICROCHIP)

S27       530   S S26 AND S3
S28       145   S S27 AND S4
S29        56   S S28 AND S6
S30        46   S S29 AND S2
S31        16   S S30 AND S8
S32        11   RD  (unique items)
S33         2   S S16 NOT S12
S34         3   S S19 NOT (S12 OR S16)
S35         0   S S22 NOT (S12 OR S16 OR S19)
S36         1   S S25 NOT (S12 OR S16 OR S19 OR S22)
S37        10   S S32 NOT (S12 OR S16 OR S19 OR S22 OR S25)
S38        33   S S24 NOT (S12 OR S16 OR S19 OR S22 OR S25 OR S32)
S39        19   RD  (unique items)
```

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact:***

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:
  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)
- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

Search and Information Resources Administration

33/9/2 (Item 1 from file: 103) **Links**
Energy SciTec

00331799 ERA-03-011852; EDB-78-020426
Author(s): Kurth, W.T.
Title: **Solar cell mounting and interconnecting assembly** (Patent)
Patent No.: US 4019924
Patent Assignee(s): Mobil Tyco Solar Energy Corp.
Patent Date Filed: Filed date 14 Nov 1975

Publication Date: 26 Apr 1977 p 10
Document Type: Patent
Language: English
Journal Announcement: EDB7802
Subfile: ERA (Energy Research Abstracts); TIC (Technical Information Center) .
Country of Origin: United States
Country of Publication: United States
Abstract: A solar cell assembly comprises a plurality of solar cells mounted on a **laminate** comprising a base **electrically-insulative sheet**, an **electrically-conductive layer** disposed on the base sheet in a predetermined pattern so as to provide **first** and **second** cell-connecting sections electrically **insulated** from **one another**, and a **second electrically-insulative sheet** having a plurality of **openings** and being disposed over the **conductive layer** so that selected portions of the **conductive layer** are exposed through the **openings**. The laminate is provided with a plurality of bent **tabs**, **each** of which includes an exposed portion of the **first** cell-connecting section so that the exposed portion can be attached to the top surface electrode of a solar cell. At least **one** exposed portion of a **second** cell-connecting section of the **conductive layer** is attached to the bottom surface electrode of the same cell. **Various circuit** patterns of the **electrically-conductive layer** are described for connecting the cells in a series or parallel array and for use in **width**-limited systems, such as solar concentrators.
Major Descriptors: ; *SOLAR CELL ARRAYS -- DESIGN; *SOLAR CELL ARRAYS -- ELECTRONIC CIRCUITS
Descriptors: DIELECTRIC MATERIALS; FABRICATION; LAMELLAE; MECHANICAL STRUCTURES; SOLAR CONCENTRATORS; SUPPORTS
Broader Terms: MECHANICAL STRUCTURES; PHOTOVOLTAIC POWER PLANTS; POWER PLANTS; SOLAR POWER PLANTS
Subject Categories: 140501* -- Solar Energy Conversion -- Photovoltaic Conversion

34/9/2 (Item 1 from file: 23) **Links**
CSA Technology Research Database

0005441939 IP Accession No: A97-15223
Thermal conductivity of multi-layer circuit boards

Lambert, M A; Fletcher, L S San Jose State Univ., CA [Lambert]
Publication Date: 1997

Conference:
AIAA, Aerospace Sciences Meeting & Exhibit, 35th, Reno, NV , UNITED STATES , 6-9 Jan. 1997

Document Type: Conference
Record Type: Abstract
Language: ENGLISH
Report No: AIAA Paper 97-0138
No. Of Refs.: 3
File Segment: Aerospace & High Technology

Abstract:
Thermal conductivity has been experimentally determined for multi-layer circuit boards. Conductivity was measured for three orthogonal directions (two inplane and one through-plane) for **several circuit** boards consisting of ten to twenty copper **conductor layers** separated by polymeric dielectric planes. Some of these **circuit boards** contain through-**holes**, called vias, to allow pins on modules to connect to interior **conductor layers**. Conductivity results were examined with respect to each other and agreed with results for standard circuit boards with conductor paths only on the top and bottom surfaces. Depending on the ratio of total metallic layer **thickness** to circuit board **thickness**, the in-plane conductivity ranged from 24.8 to 129.3 W/mK. The presence of pin holes reduced in-plane conductivity by one-third. In-plane thermal conductivity was 7 to 300 times greater than through-plane conductivity, which was 3.49 and 0.359 W/mK for circuits boards with and without pin holes, respectively. (Author)

Descriptors: *Circuit boards; ***Thermal** conductivity; ***Laminates**; *Very large scale integration; *Parameter uncertainty; Orthogonal functions; Dielectrics; Aluminum alloys
Subj Catg: 33, ELECTRONICS AND ELECTRICAL ENGINEERING

37/9/2 (Item 2 from file: 2) **Links**
Fulltext available through: custom link USPTO Full Text Retrieval Options SCIENCEDIRECT
INSPEC

07057013 **INSPEC Abstract Number:** B9812-2210D-004
Title: Limits of copper plating in high aspect ratio microvias
Author Castaldi, S.; Fritz, D.; Schaeffer, R.
Journal: CircuiTree vol.11, no.9 p. 66, 68, 72, 74
Publisher: CircuiTree ,
Publication Date: Sept. 1998 **Country of Publication:** USA
CODEN: CIRCF6 **ISSN:** 1059-843X
SICI: 1059-843X(199809)11:9L.66:LCPH;1-D
Material Identity Number: E342-98010

Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: The production of build-up multilayer **printed circuit boards** has generated enormous dialogue around the world. **Several** techniques are capable of producing microvias, such as: photolithography, where the vias are created by the action of the developer solution on the **dielectric**; plasma, where **holes** are etched in copper foil and the action of the plasma removes exposed **dielectric**; mechanical, where **dielectric** is drilled or sandblasted away; laser, using ablation to remove **both** the copper and the **dielectric**, or just the organics when "deposited **dielectric**" construction is used. All of these techniques require the metallization of the via walls to make a **conductive interconnect** between **layers** of circuitry. This article explores the capability of electroless copper deposition plus acid copper electroplating to metallize high aspect ratio microvias. Practical guidelines are given for the design geometries of laser ablated microvias. (2 Refs)
Subfile: B
Descriptors: copper; electroless deposition; electroplating; laser ablation; laser beam machining; machining; metallisation; photolithography; printed circuit manufacture; sputter etching
Identifiers: copper plating; microvias; high aspect ratio microvias; build-up multilayer printed circuit boards; photolithography; developer solution; **dielectric** materials; plasma etch; copper foil; exposed **dielectric** removal; mechanical drilling; sandblasting; laser ablation; deposited **dielectric** construction; via wall metallization; conductive **interconnect**; electroless copper deposition; acid copper electroplating; laser ablated microvias; Cu
Class Codes: B2210D (Printed circuit manufacture); B0170E (Production facilities and engineering); B0170G (General fabrication techniques); B0520 (Thin film growth); B4360 (Laser applications)
Chemical Indexing:
Cu int - Cu el (Elements - 1)

37/9/5 (Item 5 from file: 2) **Links**
INSPEC

02777804 **INSPEC Abstract Number:** B82001043
Title: Laser drilling of high density printed circuit boards
Author Klauser, H.
Author Affiliation: IBM Corp., Endicott, NY, USA
Conference Title: CLEO '81. Conference on Lasers and Electro-Optics (papers in summary form only received) p. 160
Publisher: IEEE , New York, NY, USA
Publication Date: 1981 **Country of Publication:** USA 208 pp.
Conference Date: 10-12 June 1981 **Conference Location:** Washington, DC, USA

Language: English **Document Type:** Conference Paper (PA)
Treatment: Applications (A); Experimental (X)
Abstract: During the development of a high density multilayer circuit board of large dimensions, the method eventually adopted was to use a sequential lamination technique in which planes of delicate circuit lines are built up layer by layer onto a more rugged power core. Such a concept in turn requires the capability of making electrical connections to a **conductor** buried under a **layer** of **dielectric**. Within the constraints imposed by the product design, a laser process was developed for the drilling of buried vias of 0.12 mm diameter into an epoxy/glass **dielectric** of 0.15 mm thickness. A high power CO/sub **2**/ laser was selected, as **both** epoxy and glass are strong absorbers at 10.6 mu m. The laser is operated in CW to assure the best stability with respect to power, mode structure and pointing accuracy, and debris from the drilling action was kept away by means of air flow. Four **circuit boards** are drilled simultaneously, and **several** million **holes** have been drilled and processed. Extensive testing of drilled **holes** after plating has also been done to assure a reliable **interconnection**. (0 Refs)
Subfile: B
Descriptors: carbon compounds; gas lasers; laser beam applications; printed circuits
Identifiers: laser drilling; 10.6 micron radiation; high density printed circuit boards; high density multilayer circuit board; sequential lamination technique; delicate circuit lines; electrical connections; conductor; layer of **dielectric**; drilling of buried vias; epoxy/glass **dielectric**; high power CO/sub **2**/ laser; CW; power; mode structure; pointing accuracy; debris; air flow; plating; reliable **interconnection**
Class Codes: B2210D (Printed circuit manufacture); B4320C (Gas lasers); B4360 (Laser applications)

37/9/6 (Item 6 from file: 2) **Links**
INSPEC

01452872 **INSPEC Abstract Number:** B72039367
Title: Method of forming stacked circuit boards
Inventor Hacke, H.J.
Assignee Siemens AG
Patent Number: US 3680209 **Issue Date:** 720801
Application Date: 700430
Priority Application Number: DE P1923199.3 **Priority Application Date:** 700507
Country of Publication: USA

Language: English **Document Type:** Patent (PT)
Treatment: Practical (P)
Abstract: Discloses a circuit board, which has at least **two conducting layers** separated by interposed **insulating layers**, having **electrical** connections through an **opening** in the **insulator** layer characterized by the connection having surface-to-surface bond between the **conducting layers** with a portion of at least **one conducting layer** deformed into an **opening** of the separating **insulating** layer. The **circuit board** is formed by superimposing a **plurality** of layers into a stack with the **insulating layers** between adjacent **conducting** metal **layers**. Then **heat** and pressure are applied to the stack of superimposed **layers** to force the **conducting layers** into surface-to-surface **engagement** and form the bonding of the connection. In the preferred embodiments a filler material such as a metal or metal alloy having a low melting point is provided preferably as a small **area coating** on the **conducting layers** in a pattern corresponding to the pattern of the connections. Complex circuit boards having a large number of **conducting layers** can be formed by **first** forming a core in accordance with the invention and then interposing the core between additional **insulating** and **conducting layers** and repeating the **heating** and pressing step.
Subfile: B
Descriptors: printed circuits
Identifiers: forming stacked circuit boards; **conducting layers**; interposed **insulating** layers; electrical connections; bonding; filler material; small **area** coating; core; heating; pressing; surface to surface bond
Class Codes: B2210 (Printed circuits)

1/11/2007 2:55:26 PM
1/11/2007 3:40:16 PM

[File 344] Chinese Patents Abs Jan 1985-2006/Jan
[File 347] JAPIO Nov 1976-2005/Sep(Updated 060103)
[File 350] Derwent WPIX 1963-2006/UD,UM &UP=200607
[File 371] French Patents 1961-2002/BOPI 200209

Set	Items	Description
S1	290385	S (CIRCUIT???? OR CHIP OR LOAD OR I()C OR IC OR INTEGRATED()CIRCUIT????)(3N)(BOARD OR SUBSTRATE OR WAFER????)
S2	17016767	S FIRST???? OR ONE OR 1ST OR SECOND????? OR TWO OR 2 OR BOTH OR EACH OR 2ND OR DOUBL??? OR COUPL???? OR ANOTHER OR DUAL????? OR PAIR???? OR TWIN?????
S3	721330	S (CONDUCT???? OR HEAT??? OR THERM??????? OR ELECTRIC????)(3N)(LAYER???? OR FILM???? OR COAT???? OR COVER??????? OR COVER()COAT???? OR SHEET??? OR LAMIN???? OR OVERLAY??????? OR OVER()LAY????? OR COVER()LAY??????)
S4	7176160	S INTERSTIC????? OR AREA OR SPAC???? OR REGION???? OR BREAK???? OR GAP OR GAPS OR APERTURE OR HOLE? ? OR ORIFICE? ? OR OPEN???????? OR CAVIT??????? OR PERFORAT????? OR WINDOW????
S5	1904532	S (PLURAL????? OR MANY OR MULTI?????? OR DIFFER?????? OR NUMBER?????? OR NUMEROUS OR VARI?????????? OR SEVERAL OR DIVERS?????? OR SET OR CLUSTER????)(3N)(WIDTH? ? OR BREADTH OR THICK???? OR BROAD???? OR DIMENSION OR SHAP???? OR SIZE? ?) OR WIDTH OR BREADTH OR THICK????
S6	1928547	S DIELECTRIC OR DIELEC OR CAPACIT????? OR INSULAT????? OR NONCONDUCT????? OR NON()CONDUCT????
S7	250534	S OVERHANG???? OR OVER()(HANG???? OR LAP OR LAPS OR LIES OR LIE) OR OVERLAP???? OR OVERLIE
S8	2716473	S ENGAG????? OR INTERCONNECT??? OR MESH???? OR INTERLOCK???? OR INTER()LOCK???? OR INTER()CONNECT??? OR INTERSECT???? OR JOIN???? OR LOCK????
S9	1451	S IC=(H05K-007/06)
S10	14579	S MC=(V04-R04 OR V04-V09)
S11	64	S S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7 AND S8
S12	1	S S11 AND S9
S13	3	S S11 AND S10
S14	16	S S11 AND (SEVERAL??? OR PLURAL???? OR VARI????)(3N)(CIRCUIT???? OR CHIP OR MICROCHIP OR COMPONENT OR DEVICE? ?)
S15	3	S S11 AND PARALLEL(2N)PLANE
S16	1	S S11 AND INTERSTICE(2N)ENGAG????
S17	3	S S13 NOT S12
S18	10	S S14 NOT PRINT???????
S19	10	S S18 NOT (S12 OR S13)

12/9/1 (Item 1 from file: 350) **Links**
Derwent WPIX

0006575150 *Drawing available*
WPI Acc no: 1993-386913/
XRPX Acc No: N1993-298781

Structure for packaging IC devices on multi-chip modules - has chip secured to substrate and electrically connected and subsequent chips stacked to desired height

Patent Assignee: NCHIP INC (NCHI-N)
Inventor: BRATHWAITE N E; FLATOW K; MARELLA P; TUCKERMAN D B

Patent Family (3 patents, 40 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1993023982	A1	19931125	WO 1993US4416	A	19930510	199348	B
AU 199342426	A	19931213	AU 199342426	A	19930510	199413	E
US 5804004	A	19980908	US 1992881452	A	19920511	199843	E
			US 1994300575	A	19940902		
			US 1996655338	A	19960524		

Alerting Abstract WO A1
The structure is for stacking IC chips (150a-150c). A **first** chip is secured to a silicon **circuit board** (160) with a layer of adhesive (170), and the others with an interstitial **layer** of **thermally conductive** and electrically **non-conductive** adhesive (188). Electrical connection is made via wires (189,190) to bond pads (180,192).
In fabrication, the **first** chip is secured to the **circuit board**, and wire-bonded to the bond pads (18), which provide contacts through vias for connection to **interconnect layers** (182) and **conducting** plane (183) containing power, and ground planes (184,186) of the silicon **circuit board**. **Each chip** is stacked and similarly connected to respective bond pads, which may be staggered to facilitate wire removal if necessary.
ADVANTAGE - Provides structure for reducing **size** and complexity of **multi**-chip modules with less cost and technological risk.

Title Terms /Index Terms/Additional Words: STRUCTURE; PACKAGE; IC; DEVICE; MULTI; CHIP; MODULE; SECURE; SUBSTRATE; ELECTRIC; CONNECT; SUBSEQUENT; STACK; HEIGHT; INTEGRATED; CIRCUIT

Claim:

1. A method for fabricating a multichip module comprising the steps of:
   - attaching a first integrated circuit having a bonding pad region to a surface of a silicon circuit board;
   - wire bonding a conductor between said bonding pad region of said first integrated circuit and a first set of bond pads located on said circuit board;
   - placing a layer of adhesive atop said first integrated circuit;
   - placing a second integrated circuit having a recessed bottom surface along a bottom edge of said second integrated circuit atop said layer of adhesive wherein at least a portion of said recessed bottom surface of

said second integrated circuit overhangs said bonding pad region of said first integrated circuit; and

- wire bonding a conductor between said bonding pad region of said second integrated circuit and a second set of bond pads located on said circuit board.

17/9/2 (Item 2 from file: 350) **Links**
Derwent WPIX

0008745263
WPI Acc no: 1998-287445/
XRAM Acc no: C1998-089141
XRPX Acc No: N1998-225930
Multilayer circuit board interconnection method - by laminating boards after aligning their conductive pads using flexible Z-axis selectively conductive material containing adhesive
Patent Assignee: GORE & ASSOC INC W L (GORE)
Inventor: MEOLA C G; SUILMANN D M

Patent Family (2 patents, 74 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1998020715	A1	19980514	WO 1997US18992	A	19971022	199825	B
AU 199749113	A	19980529	AU 199749113	A	19971022	199841	E

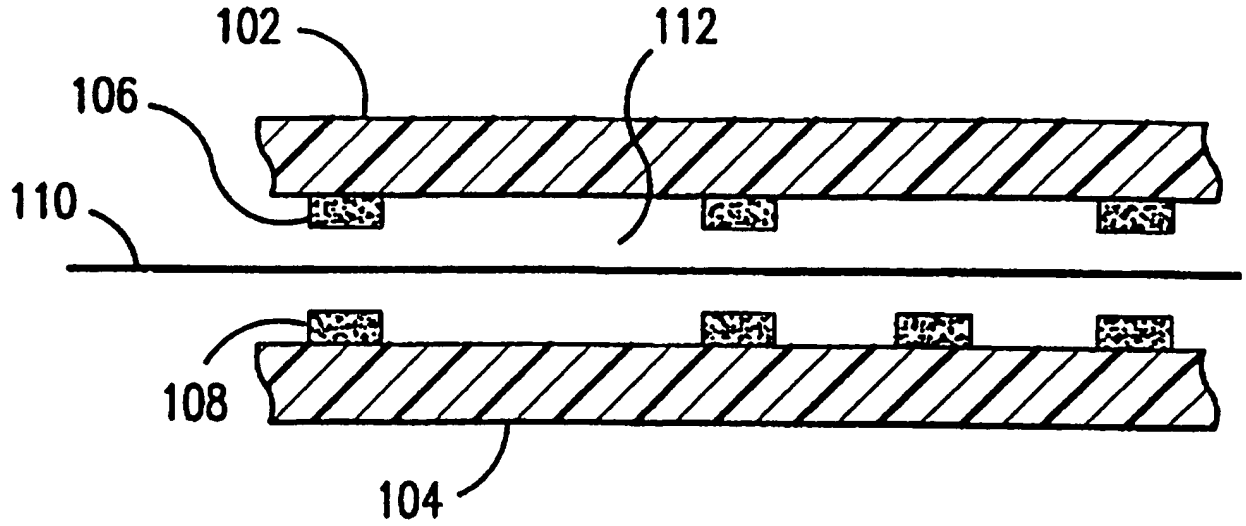
Alerting Abstract WO A1
A method of **interconnecting** printed circuit boards comprises: (a) providing **2** circuit boards (102, 104) having conductive pads (106, 108) on their faces and aligning conductive pads to be **interconnected** opposite **each** other; (b) providing between opposing faces of the **circuit board**, a Z-axis conductive member (110) comprising a planar, **open** cell, porous material with a series of electrically isolated, vertically defined cross-sectional areas (114), which extend from **one** side of the material to the other, the material being **covered** with a **conductive** metal and containing an adhesive in the porous material; and (c) laminating the **2** circuit boards with the Z-axis conductive member such that the conductive pads are connected electrically by the Z-axis conductive member.
USE - For forming assemblies of printed circuit boards (claimed).
ADVANTAGE - The method fills interstitial void **spaces**, preventing process chemicals from being trapped in them and causing corrosion and improving the reliability of the **interconnection**. The Z-axis conductive material is sufficiently compressible and compliant to fill interstitial **gaps** and the surface metallisation provides lower contact resistance and better uniformity of signal quality than a material that uses conductive particles. The method may be used to laminated boards of **different sizes** (claimed), and smaller boards may be laminated only in areas where they are required, which reduces costs and allow the composite to be thinner in areas where there is a tight clearance. Boards having 4-5 mil diameter pads on 8-10 mil centres may be **interconnected** and the porous materials have relatively low moduli, which provides stress decoupling between the **interconnected** boards.

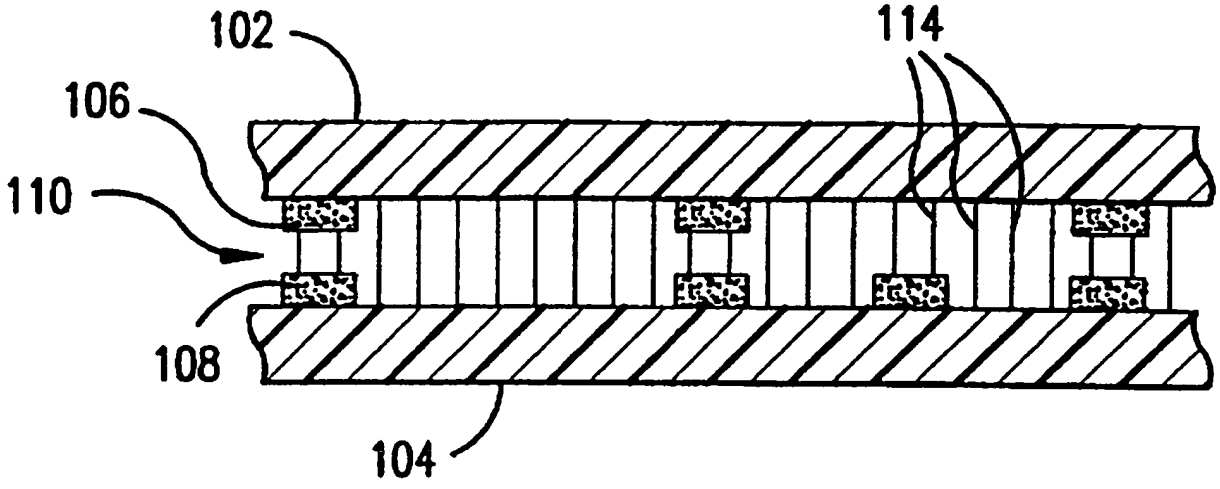
Documentation Abstract
A method of **interconnecting** printed circuit boards comprises: (a) providing **2** circuit boards (102, 104) having conductive pads (106, 108) on their faces and aligning conductive pads to be **interconnected** opposite **each** other; (b) providing between opposing faces of the **circuit board**, a Z-axis conductive member (110) comprising a planar, **open** cell, porous material with a series of electrically isolated, vertically defined cross-sectional areas (114), which extend from **one** side of the material to the other, the material being **covered** with a **conductive** metal and containing an adhesive in the porous material; and (c) laminating the **2** circuit boards with the Z-axis conductive member such that the conductive pads are connected electrically by the Z-axis conductive member.
USE - For forming assemblies of printed circuit boards (claimed).

ADVANTAGE - The method fills interstitial void **spaces**, preventing process chemicals from being trapped in them and causing corrosion and improving the reliability of the **interconnection**. The Z-axis conductive material is sufficiently compressible and compliant to fill interstitial **gaps** and the surface metallisation provides lower contact resistance and better uniformity of signal quality than a material that uses conductive particles. The method may be used to laminated boards of **different sizes** (claimed), and smaller boards may be laminated only in areas where they are required, which reduces costs and allow the composite to be thinner in areas where there is a tight clearance. Boards having 4-5 mil diameter pads on 8-10 mil centres may be **interconnected** and the porous materials have relatively low moduli, which provides stress decoupling between the **interconnected** boards.

PREFERRED METHOD - At least 3 circuit boards are provided. The conductive pads may project from the face of the **circuit board** or be recessed from the face, or **one** board may have projecting pads and **another** board recessed pads. **One** board may be smaller than the other, or **one** may partially **overlap** the other. The porous material is a polymer, e.g. a polyolefin, preferably porous polypropylene or polyethylene or a fluoropolymer, preferably porous expanded polytetrafluoroethylene (ePTFE), a porous copolymer of PTFE, e.g. a copolymer containing polyester or polystyrene, a porous copolymer of fluorinated ethylene-propylene or a porous copolymer of perfluoroalkoxy tetrafluoroethylene (PFA) containing a 1-4C alkoxy group. The conductive metal is copper, nickel, gold or a mixture. The adhesive is an epoxy, acrylic, urethane, silicone, polyimide or cyanate-ester resin. An electronic device may be attached to the **circuit board** assemblies, e.g. a resistor, **capacitor**, inductor, semiconductor , transistor, diode, integrated circuit, microprocessor, memory or logic device, analogue-to-digital converter, digital-to-analogue converter, amplifier, filter, modulator, demodulator or peak detector. The material has a **thickness** of 5-500 mumb (50-125 mum).

EXAMPLE - A layer of a stretched porous PTFE membrane having the node-fibril structure of **thickness** 76 mum, density 0.22 g/cm^3 and air volume 70% at 25(deg)C was used to form a Z-axis membrane. It was made receptive to metal deposition by treating selected areas with a liquid, UV radiation-sensitive composition comprising a light-sensitive reducing agent, a metal salt, a source of halide ions and a **second** reducing agent for 5-15 min to allow the liquid to penetrate the pores of the material and form a coating defining the pores from **one** side to the other. The membrane was dried, **both** surfaces were masked with **2** mil pads with a 5 mil pitch and the membrane was exposed to UV radiation under conditions of time and power sufficient to reduce the metal cations to metal throughout the **thickness** of the membrane. The masking was then removed and the unexposed composition was washed from the membrane with an acidic or alkaline solution. If a washing time of 5 min or less is used, the process has no effect on the metal formed above. A reactive metallic cation replacement solution was used to replace the metal atoms with more stable metallic cations, e.g. Pd or Au. The membrane was then plated electrolessly using a solution of a conductive metal, e.g. Ni, Au, Cu or a combination, and dried. A Z-axis conductive scaffolding was formed in the areas that had not been masked. The pores of the membrane were then filled with adhesive by immersing it in a solution of the adhesive resin, e.g. in methyl ethyl ketone.





(KR)

Title Terms /Index Terms/Additional Words: MULTILAYER; CIRCUIT; BOARD; **INTERCONNECT**; METHOD; LAMINATE; AFTER; ALIGN; CONDUCTING; PAD ; FLEXIBLE; Z-AXIS; SELECT; MATERIAL; CONTAIN; ADHESIVE

17/9/3 (Item 3 from file: 350) **Links**
Derwent WPIX

0007896674
WPI Acc no: 1996-187152/199619
Related WPI Acc No: 1989-371878
XRAM Acc no: C1996-059760
XRPX Acc No: N1996-156595

Electrically and mechanically interconnecting conductive layers having aligned interconnecting pads using adhesive - contg. dispersed deformable conductive metallic particles, the assembled layers being clamped and heated to cure the adhesive matrix and allow the particles to form conductive bridges across its thickness

Patent Assignee: SHELDAHL INC (SCJE)
Inventor: CASSON K L; GILLEO K B; MAHAGNOUL E; MYERS C; SUILMANN D; TIBESAR M

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5502889	A	19960402	US 1988206086	A	19880610	199619	B
			US 1992925954	A	19920805		
			US 19931811	A	19930108		
US 5688584	A	19971118	US 1988206086	A	19880610	199801	E
			US 1992925954	A	19920805		
			US 19931811	A	19930108		
			US 1995534630	A	19950927		

Alerting Abstract US A

At least **two conductive layers** (72,76), **each** having a conductive pattern and contact pads on it including at least **one interconnecting** pad (74) corresponding to an **interconnecting** pad (79) on **another conductive layer** and at least **one** of which is affixed to an **insulating** substrate, are electrically and mechanically connected together by **layering electrically interconnecting** adhesive (85) over a portion of at least **one** of them to form an **interconnecting** layer, aligning the other with it so that their **interconnecting** pads are aligned, and heating the assembly while applying clamping pressure to form an **interconnected** assembly in which the **interconnecting** pads are aligned, and heating the assembly while applying clamping pressure to form an **interconnected** assembly in which the **interconnecting** assembly is conductive across its **thickness** but not in a co-planar direction. The **interconnecting** adhesive is a **non-conductive** thermosetting adhesive (86) having deformable metallic particles (87,92) dispersed uniformly throughout it such that **each** particle is electrically **insulated** from every other particle until pressure is applied, particles and **insulating** substrate having similar coefficients of thermal expansion. The particles have a maximum dia. that is 90-110 percent of the distance between the **conductive layers** but the adhesive includes deformable conductive metallic particles of smaller dia. also.

USE - Method is used to fabricate multi-layer electronic circuits.

ADVANTAGE - Method enables less complex fabrication and provides connections between **conductive layers** which are less susceptible to thermal stress because the **interconnecting** metallic particles have a thermal expansion coefficient similar to that of the **insulating** substrate.

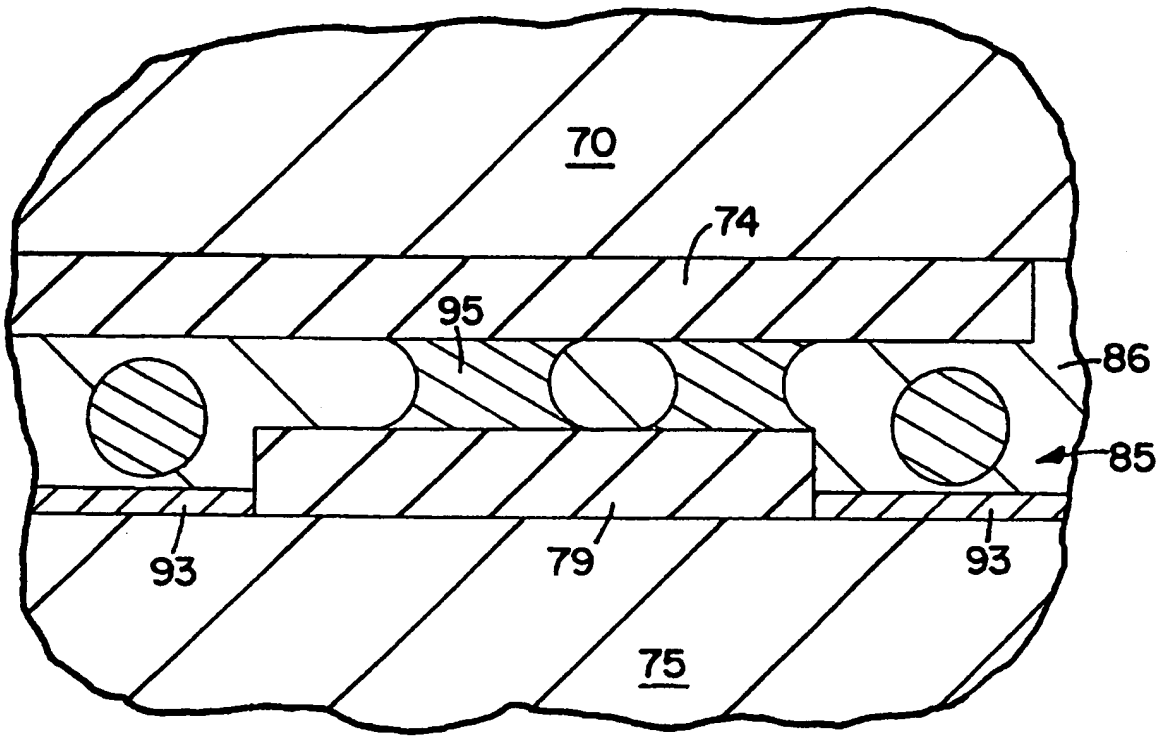
Documentation Abstract

At least **two conductive layers** (72,76), **each** having a conductive pattern and contact pads on it including at least **one interconnecting** pad (74) corresponding to an **interconnecting** pad (79) on **another conductive layer** and at least **one** of which is affixed to an **insulating** substrate, are electrically and mechanically connected together by **layering electrically interconnecting** adhesive (85) over a portion of at least **one** of them to form an **interconnecting** layer, aligning the other with it so that their **interconnecting** pads are aligned, and heating the assembly while applying clamping pressure to form an **interconnected** assembly in which the **interconnecting** pads are aligned, and heating the assembly while applying clamping pressure to form an **interconnected** assembly in which the **interconnecting** assembly is conductive across its **thickness** but not in a co-planar direction. The **interconnecting** adhesive is a **non-conductive** thermosetting adhesive (86) having deformable metallic particles (87,92) dispersed uniformly throughout it such that **each** particle is electrically **insulated** from every other particle until pressure is applied, particles and **insulating** substrate having similar coefficients of thermal expansion. The particles have a maximum dia. that is 90-110 percent of the distance between the **conductive layers** but the adhesive includes deformable conductive metallic particles of smaller dia. also.

USE - Method is used to fabricate multi-layer electronic circuits.

ADVANTAGE - Method enables less complex fabrication and provides connections between **conductive layers** which are less susceptible to thermal stress because the **interconnecting** metallic particles have a thermal expansion coefficient similar to that of the **insulating** substrate.

PREFERRED METHOD - Before **layering** the adhesive, an **electrically insulating cover layer** (93), having apertures corresponding to the **interconnecting** pads of **one** of the **conductive layers**, is aligned with **one** of the layers. Before alignment, the **interconnecting** layer is dried to form a B stage adhesive, the drying being carried out in a conveyor oven at 220-250 (deg)F for a dwell time of 10 minutes. The layering is performed by screen printing. The assembly is heated and pressed in a platen press at 380 (deg)F and 300 psi for 50 minutes. The conductive particles are spherical. 80 percent of them have a dia. within 20 percent of a mean dia. They are made of eutectic solder composed of 63 parts tin and 37 parts lead, more pref., 62.5 parts tin, 36.1 parts lead, and 1.4 parts silver. The coefficients of thermal expansion of the particles and the **insulating** substrate are within 25 percent. The dia. of the apertures in the cover layer is such that the ratio of that dia. to the distance between connected layers optimises **interconnection** between opposed **interconnecting** pads, the ratio esp. being 25:1, the **aperture** dia. being 1250 microns and the connected distance 50 microns. **Each conductive layer** is affixed to an **insulating** substrate which is rigid ceramic, resin, or glass epoxy. At least **one** substrate is flexible polyimide or polyester. The substrates are 12.5-125 microns **thick**, the **conductive layers** 5-140 microns **thick**, and the **interconnecting** layer 15-100 microns.



(JP)

Title Terms /Index Terms/Additional Words: ELECTRIC; MECHANICAL; **INTERCONNECT**; CONDUCTING; LAYER; ALIGN; PAD; ADHESIVE; CONTAIN; DISPERSE; DEFORM; METALLIC; PARTICLE; ASSEMBLE; CLAMP; HEAT; CURE; MATRIX; ALLOW; FORM; BRIDGE; **THICK**

Claim:

1. A method for electrically and mechanically connecting at least two conductive layers, each conductive layer having a conductive pattern and a plurality of contact pads defined thereon, and at least one contact pad being designated an interconnecting pad, each interconnecting pad on a conductive layer having a corresponding interconnecting pad on another conductive layer, at least one conductive layer affixed to an insulating substrate, the method comprising the steps of: layering an electrically interconnecting adhesive over a portion of one of the at least two conductive layers to form an interconnecting layer, the interconnecting adhesive comprising a non-conductive thermosetting adhesive having a first plurality of deformable conductive metallic particles dispersed substantially uniformly throughout the non-conductive adhesive such that each particle is electrically insulated from substantially every other particle, the particles and the insulating substrate having substantially similar coefficients of thermal expansion, the particles having a maximum diameter that is about 90-110% of a distance between the conductive layers, the interconnecting adhesive further including a second plurality of deformable conductive metallic particles having a diameter smaller than the first plurality of particles; aligning the other of the at least two conductive layers to form an uncured assembly, such that the interconnecting layer is interposed between the at least two conductive layers with the interconnecting pads on each conductive layer aligned with their corresponding pads on the other conductive layer; and subjecting the uncured assembly to an elevated temperature and a clamping pressure to form an interconnected assembly, such that the interconnecting layer becomes conductive across a thickness thereof and non-conductive throughout a coplanar direction thereof, and such that the two conductive layers are mechanically connected in a superposed relationship with a

connected distance therebetween and corresponding interconnecting pads on the two conductive layers are electrically connected.

FOR YOUR INFORMATION

19/9/1 (Item 1 from file: 350) **Links**
Derwent WPIX

0015580296 *Drawing available*
WPI Acc no: 2006-144460/200615
Related WPI Acc No: 2006-413751
XRAM Acc no: C2006-048895
XRPX Acc No: N2006-124932
Semiconductor chip for multichip packaging has semiconductor substrate with upper and lower faces, outer edge and at least first contact pad, electrically insulating region with through hole and connection electrode
Patent Assignee: CHUNG H (CHUN-I); JANG D (JANG-I); LEE I (LEEI-I); PARK M (PARK-I); SAMSUNG ELECTRONICS CO LTD (SMSU); SIM S (SIMS-I); SONG Y (SONG-I)
Inventor: CHO T; CHUNG H; CHUNG H S; JANG D; LEE I; LEE I Y; PARK M; PARK M S; SIM S; SIM S M; SONG Y; SONG Y H; JANG D H

Patent Family (5 patents, 5 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20060019467	A1	20060126	US 2005147677	A	20050608	200615	B
JP 2006041512	A	20060209	JP 2005204665	A	20050713	200615	E
DE 102005036646	A1	20060323	DE 102005036646	A	20050727	200622	E
CN 1728370	A	20060201	CN 200510087557	A	20050727	200639	E
KR 2006010099	A	20060202	KR 200458689	A	20040723	200660	E

Alerting Abstract US A1
NOVELTY - A semiconductor **chip** comprises a semiconductor **substrate** having upper and lower faces that extend to an outer edge of the substrate and at least a **first** contact pad on a portion of the upper face extending adjacent the outer edge; an electrically **insulating region** on the outer edge of the substrate and having a through **hole**; and a connection electrode extending through the through **hole** and electrically connected to the **first** contact pad.
DESCRIPTION - INDEPENDENT CLAIMS are also included for:

1. a method of fabricating integrated circuit chips, comprising forming criss-crossing grooves (37) in a semiconductor wafer (30) having contact pads (31); filling the criss-crossing grooves with an electrically **insulating layer** (38); patterning the **electrically insulating layer** to define at least **first** and **second** through-**holes** (41) that extend in a **first one** of the criss-crossing grooves; filling the **first** and **second** through-**holes** with **first** and **second** through-chip connection electrodes, respectively; and dicing the semiconductor **wafer** into **integrated circuit** chips by cutting through the **electrically insulating layer** in a cross-crossing pattern that **overlaps** with the locations of the criss-crossing grooves; and
2. a method of processing a semiconductor wafer, comprising forming criss-crossing grooves in the semiconductor wafer; filling the criss-crossing grooves with an **electrically insulating layer**; removing an underside of the semiconductor wafer to expose a surface of the **electrically insulating layer** having a cross-crossing pattern; and dicing the semiconductor **wafer** into **integrated circuit** chips having electrically **insulating** edges by

cutting through the electrically **insulating region** at locations defined by the criss-crossing pattern.

USE - For multichip packaging.
ADVANTAGE - The chip provides reliable **interconnection** vias when the chip is used in stacked multichip packaging applications.
DESCRIPTION OF DRAWINGS - The figure is a cross-section of an intermediate structure formed during fabrication of integrated circuit chips.
30 Semiconductor wafer
31 Contact pads
32 Semiconductor substrate
37 Criss-crossing grooves
38 **Electrically insulating layer**
41 **First** and **second** through-**holes**
42 Base metal layer
52 **Opening**

Technology Focus
ELECTRONICS - Preferred Component: The **electrically insulating layer** has a lower surface that is coplanar with the lower face of the semiconductor substrate (32). A length of the through-**hole** is greater than a **thickness** of the semiconductor substrate. A longitudinal axis of the through-**hole** is parallel to the outer edge of the semiconductor **substrate**. The semiconductor **chip** further comprises a passivation layer extending on the upper face and having an **opening** (52) that exposes the **first** contact pad, and a solder bump electrically connected to a portion of the connection electrode extending adjacent a bottom of the through-**hole** . The electrically **insulating region** wraps around the outer edge and extends onto the passivation layer. It extends between the upper face and the connection electrode. An outer edge of the electrically **insulating region** represents an outer edge of the semiconductor chip. Preferred Method: The dicing step is preceded by a step of removing an underside of the semiconductor wafer to expose the **first** and **second** through chip connection electrodes and the **electrically insulating layer**. The step of filling the **first** and **second** through-**holes** includes depositing a base metal layer (42) that extends on the **electrically insulating layer** and lines the **first** and **second** through **holes**; electroplating the **first** and **second** through chip connection electrodes into the **first** and **second** through **holes**; and etching back the base metal layer using the **first** and **second** through chip connection electrodes as an etching mask. The electroplating step includes electroplating the **first** and **second** through chip connection electrodes into the **first** and **second** through **holes** using the base metal layer as an electroplating electrode. It is preceded by a step of patterning an electroplating mask on the base metal layer. The removing step is preceded with the steps of forming the through **holes** in the **electrically insulating layer**, and filling the through **holes** with corresponding connection electrodes. It includes removing the underside of the semiconductor wafer to expose a surface of the **electrically insulating layer** and the connection electrodes.

Title Terms /Index Terms/Additional Words: SEMICONDUCTOR; CHIP; PACKAGE; SUBSTRATE; UPPER; LOWER; FACE; OUTER; EDGE; **FIRST**; CONTACT; PAD; ELECTRIC; **INSULATE**; **REGION**; THROUGH; **HOLE**; CONNECT; ELECTRODE

Claim: That which is claimed is:

3. **1**. A semiconductor chip, comprising:
- a semiconductor substrate having upper and lower faces thereon that extend to an outer edge thereof and at least a first contact pad on a portion of the upper face extending adjacent the outer edge;
- an electrically insulating region on the outer edge of said semiconductor substrate, said electrically

insulating region having through-hole therein; and

- a connection electrode that extends through said through-hole and is electrically connected to the first contact pad.

(FILE 'HOME' ENTERED AT 16:11:45 ON 11 JAN 2007)

FILE 'CAPLUS' ENTERED AT 16:12:01 ON 11 JAN 2007

L1 85793 SEA ABB=ON PLU=ON (CIRCUIT#### OR IC OR I C OR LOAD OR PRINT###### OR INTEGRATED CIRCUIT#### OR CHIP OR FLEX####)(3A)(BOARD OR SUBSTRATE)

L2 2085316 SEA ABB=ON PLU=ON INTERSTIC###### OR HOLE OR GAP OR SPAC##### OR BREAK#### OR CAVIT###### OR APERTUR#### OR ORIFIC###### OR OPEN######## OR PERFORAT####

L3 335280 SEA ABB=ON PLU=ON DIELEC OR DIELECTRIC

L4 116481 SEA ABB=ON PLU=ON (SEVERAL OR MULTI######## OR MANY OR PLURAL###### OR VARI########)(3A)(CHIP OR COMPONENT OR DEVICE OR CIRCUIT####)

L5 595722 SEA ABB=ON PLU=ON CAPACIT########

L6 1726808 SEA ABB=ON PLU=ON WIDTH OR BREADTH OR BROAD#### OR DIMENSION### OR THICK#####

L7 225138 SEA ABB=ON PLU=ON ENGAG#### OR INTERLOCK###### OR INTERCONNECT###### OR MESH#### OR INTERSECT######

L8 114665 SEA ABB=ON PLU=ON OVERLAP#### OR OVERHANG########

L9 157 SEA ABB=ON PLU=ON S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7 AND S8

L10 225 SEA ABB=ON PLU=ON S1(3A)S4(3A)S3

L11 0 SEA ABB=ON PLU=ON L10 AND CONDUCT###(3A)LAYER######

L12 4981 SEA ABB=ON PLU=ON L1 AND CONDUCT####(3A)LAYER####

L13 21 SEA ABB=ON PLU=ON L12 AND L2 AND L3 AND L5 AND L4

L14 8 SEA ABB=ON PLU=ON L13 AND L7

L15 0 SEA ABB=ON PLU=ON L13 AND L8

D L14 IBIB ABS 1-8

L16 13 SEA ABB=ON PLU=ON L13 NOT L14

D L16 IBIB ABS 1-13

FILE 'STNGUIDE' ENTERED AT 16:25:28 ON 11 JAN 2007

L16 ANSWER 8 OF 13 CAPLUS COPYRIGHT 2007 ACS on STN
ACCESSION NUMBER: 1998:779775 CAPLUS
DOCUMENT NUMBER: 130:59766
TITLE: Multilayer wiring board
INVENTOR(S): Kume, Kenji
PATENT ASSIGNEE(S): Kyocera Corp., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10322029	A	19981204	JP 1997-132152	19970522
PRIORITY APPLN. INFO.:			JP 1997-132152	19970522

AB A multilayer wiring board is described, which comprises a number of organic resin insulator layers and thin-film wiring ***conductor layers*** connected via through ***holes*** in the resin insulator layers. A ***capacitor*** of an organic ***dielec***. layer between ***capacitor*** electrodes is provided in a ***hole*** in one of the organic resin insulator layers. Specifically, the organic ***dielec***. layer may comprise Ba titanate, Sr titanate, Ca titanate, Mg titanate, Cu, Al, As, Au, Ag, Mo, and/or W. The wiring board is useful for electronic packaging.

L16 ANSWER 11 OF 13 CAPLUS COPYRIGHT 2007 ACS on STN
ACCESSION NUMBER: 1997:562970 CAPLUS
DOCUMENT NUMBER: 127:241936
TITLE: Thin-film ***multilayer circuit boards*** and fabrication thereof
INVENTOR(S): Someta, Hiroki
PATENT ASSIGNEE(S): Fujitsu Ltd., Japan
SOURCE: Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09219587	A	19970819	JP 1996-22907	19960209
PRIORITY APPLN. INFO.:			JP 1996-22907	19960209

AB The title ***circuit boards*** have via-***hole***-formed polymer interlayer insulators and circuit ***conductive layers*** which are alternately laminated to give ***multilayer circuit boards***. The title fabrication involves replacing desired portions of the insulator layers with a composite oxide high-***dielec***. film and subsequently laser annealing the ***dielec***. film selectively. The fabrication provides ***dielec***. films and elec. ***capacitors*** by the ***dielec***. films bound between upper and lower ***conductive layers***.